General Description

The iP5970 is a high-performance video controller integrating Audio codec and providing video streaming,H264 by SPI interface. SPI interface is suitable for 8/16/32 bit MCU applications especial for 32bit Cotex M series,e.g. M0,M3,M4,M7 or Cotex M based SoC like IoT WiFi SoC, MT7687,MT7686. It supports various VGA CMOS sensors (640 X 480 pixels) and contains H264 compression encoders to reduce data volume. The iP5970 is equipped excellent 16bit sigma-delta audio codec to provide good 2-way audio experience. The 2 way audio function can be implemented by I^2S connecting to SoC. There is another way for audio-in (Micro phone) if need audio-in function only. It is that audio-in data can accompany with video streaming delivery by SPI. It provides I^2C,UART interfaces and general I/O. The general I/O can implement PT (Pan & Tilt) functions by external ADC driver for movement. In H264 encoder, iP5970 performs excellent bit rate control methods,CBC & VBC, to meet internet limit bandwidth and constant image quality requirements. In Windows software tool, USB is used for debugging or tuning color of sensors mode, The advantage of SPI video interface does not need OS driver and is an easy way to implement camera function for IoT products.

The iP5970 is equipped image enhance engine and noise reduction to achieve good image quality. Simple OSD function is useful to note camera number in multi camera system. Motion detection function is a simple way to detect object's movement.

Overall, the iP5970 presents excellent image quality, low bit rate and offers many useful functions. It does not need external SDRAM / DDR memory and need few components to realize compact board size. It owns good EMI-free character due to hardwired design. Therefore, iP5970 is really a video co-processor with high CP ratio. In mobile era, WiFi & Bluetooth & 3G/4G are interfaces to mobile devices, mobile phone, tablet PC. iP5970 can make WiFi /BT /3G/4G device is eqipped with camera function easilly for IoT applications.

Features

- Support VGA CMOS sensors :
  - ON(Aptina) : ASX340,MT9V139
  - Ominivision : OV7740, OV7725
  - Pixart : PAS6329,PAS7366
  - GalaxyCore : GC0328
- Support sensor output : YUV, CCIR656
- Support Progressive Video Decoder
  - ADV7280
  - TW9912
- Video output : SPI video interface
  - SPI : data rate Up to Max. 40MHz
  - Support Master / Slave mode
  - 30fps @VGA in H264
- Provide 16bit Audio Codec
  - 16bit sigma-delta ADC
    - Sample rate (HZ): 8K ~ 16K,
    - Support Microphone
    - Excellent audio quality SNR up to 92dB
    - Output interface : SPI or I^2S accompanying with video stream
    - Output data format : PCM
  - 16bit sigma-delta DAC
    - Support Mute function up to -100dB
    - Support Volume Control
    - SNR up to 100dB to perform excellent audio quality
    - Sample rate (HZ) : 8K ~ 48K
- Provide I^2S for 2 way Audio (Audio in/out)
- Provide time-lapse function
- H264 Encoder supported
  - Baseline profile : 30fps @VGA (640 x 480)
  - Support CAVLC entropy encoding
  - Support CBC & VBC bit rate control
- Provide video streaming H264
  - 30fps @ VGA(640 x 480) resolution in Maximum
- Provide RTC interface for external RTC chip for

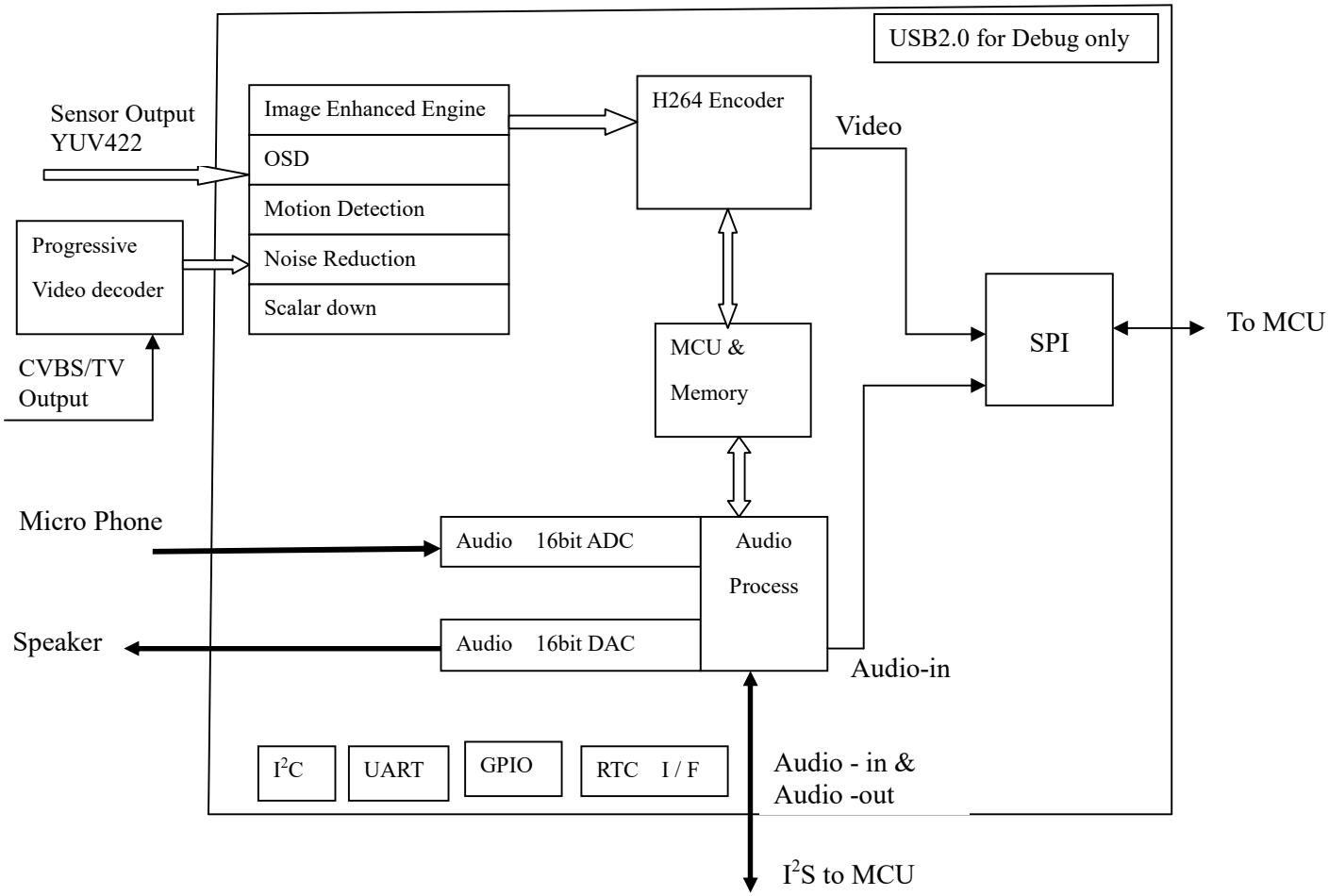
time stamp

- Built-in simple OSD to customize message
- Enhanced image enhancement engine
- Noise reduction supported to improve image quality
- Provide Motion Detection function
- Provide image scaling down function
- Provide UART, I^2C and General I/O
- No external SDRAM / DDR memory
- 88-pin QFN package (10 X 10 mm^2)

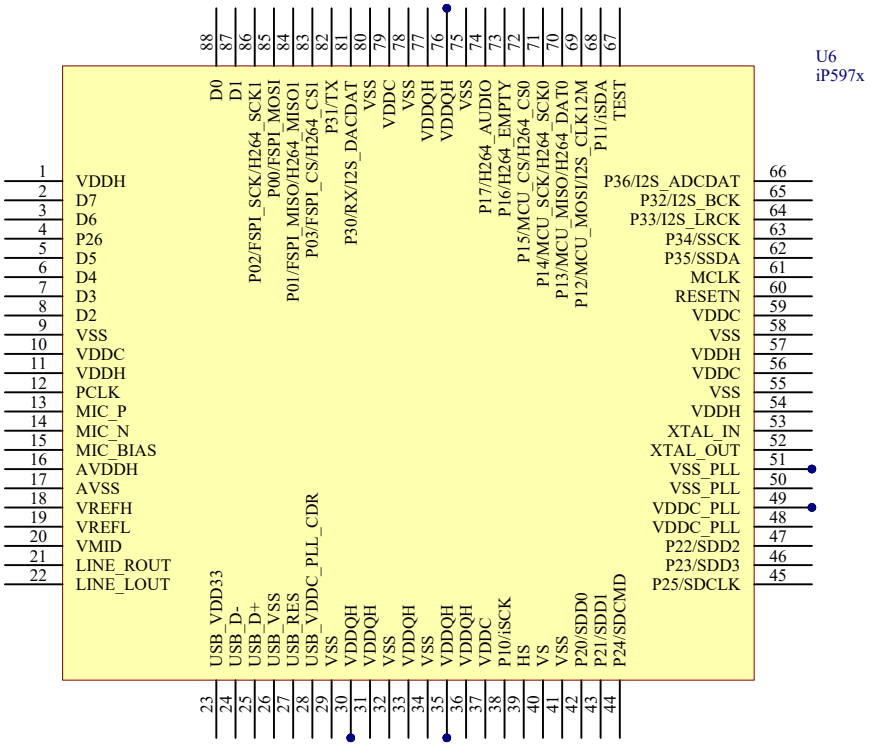
Applications

- Battery-powered Home Security WiFi / Wireless Camera
- Battery-powered Baby Monitor WiFi Camera
- WiFi / Wireless Door Phone
- Battery-powered WiFi Pet Camera
- Battery-powered WiFi vehicle camera
- Battery-powered video products of IoT applications

- **Block Diagram**



Pin Diagram


U6
iP597x
1 VDDH
2 D7
3 D6
4 P26
5 D5
6 D4
7 D3
8 D2
9 VSS
10 VDDC
11 VDDH
12 PCLK
13 MIC_P
14 MIC_N
15 MIC_BIAS
16 AVDDH
17 AVSS
18 VREFH
19 VREFL
20 VMID
21 LINE_ROUT
22 LINE_LOUT
23 USB_VDD33
24 USB_D-
25 USB_D+
26 USB_VSS
27 USB_RES
28 USB_VDDC_PLL_CDR
29 VSS
30 VDDQH
31 VDDQH
32 VSS
33 VDDQH
34 VSS
35 VDDQH
36 VDDQH
37 VDDC
38 P10/iSCK
39 HS
40 VS
41 VSS
42 P20/SDD0
43 P21/SDD1
44 P24/SDCMD
45 P25/SDCLK
46 P23/SDD3
47 P22/SDD2
48 VDDC_PLL
49 VDDC_PLL
50 VSS_PLL
51 VSS_PLL
52 XTAL_OUT
53 XTAL_IN
54 VDDH
55 VSS
56 VDDC
57 VDDH
58 VSS
59 VDDC
60 RESETN
61 MCLK
62 P35/SSDA
63 P34/SSCK
64 P33/I2S_LRCK
65 P32/I2S_BCK
66 P36/I2S_ADCDAT
67 TEST
68 P11/iSDA
69 P12/MCU_MOSI/I2S_CLK12M
70 P13/MCU_MISO/H264_DAT0
71 P14/MCU_SCK/H264_SCK0
72 P15/MCU_CS/H264_CS0
73 P16/H264_EMPTY
74 P17/H264_AUDIO
75 VSS
76 VDDQH
77 VDDQH
78 VSS
79 VDDC
80 VSS
81 P30/RX/I2S_DACDAT
82 P31/TX
83 P03/FSPI_CS/H264_CS1
84 P01/FSPI_MISO/H264_MISO1
85 P00/FSPI_MOSI
86 P02/FSPI_SCK/H264_SCK1
87 D1
88 D0

Pin Description

No.	Name	Attr.	Description
1	VDDH	P	Digital power 3.3V
2	D7	I	Sensor Data : D7
3	D6	I	Sensor Data: D6
4	P26	IO	General purpose IO
5	D5	I	Sensor Data : D5
6	D4	I	Sensor Data : D4
7	D3	I	Sensor Data : D3
8	D2	I	Sensor Data : D2
9	VSS	P	Digital power ground
10	VDDC	P	Digital core power 1.2V
11	VDDH	P	Digital power 3.3V
12	PCLK	I	Pixel clock from sensor
13	MIC_P	I	Analog MIC differential or single-ended input
14	MIC_N	I	Analog MIC differential input
15	MIC_BIAS	O	MIC bias output
16	AVDDH	P	Analog power 3.3V
17	AVSS	P	Analog power ground
18	VREFH	I	Analog positive reference 3.3V
19	VREFL	I	Analog negative reference
20	VMID	I	Mid-rail reference decoupling point
21	LINE_ROUT	O	Right channel line output
22	LINE_LOUT	O	Left channel line output
23	USB_VDD33	P	Power 3.3V
24	USB_D-	B	USB differential signal, DN
25	USB_D+	B	USB differential signal, DP
26	USB_VSS	P	Digital power ground
27	USB_RES	P	A reference for the current resource of USB
28	USB_VDDC _PLL_CDR	P	Power 1.2V
29	VSS	P	Digital power ground
30	VDDQH	P	Built-in Memory Power 3.3V
31	VDDQH	P	Built-in Memory Power 3.3V
32	VSS	P	Digital power ground
33	VDDQH	P	Built-in Memory Power 3.3V

34	VSS	P	Digital power ground
35	VDDQH	P	Built-in Memory Power 3.3V
36	VDDQH	P	Built-in Memory Power 3.3V
37	VDDC	P	Digital core power 1.2V
38	P10 / iSCK	B	General purpose IO iP597x Slave I2C Clock
39	HS	I	HSYNC of sensor data
40	VS	I	VSYNC of sensor data
41	VSS	P	Digital power ground
42	P20 / SDD0	B	General purpose IO SD data0
43	P21 / SDD1	B	General purpose IO SD data1
44	P24 / S DCMD	B	General purpose IO SD command
45	P25 / SD CLK	B	General purpose IO SD clock
46	P23 / SDD3	B	General purpose IO SD data3
47	P22 / SDD2	B	General purpose IO SD data4
48	VDDC_PLL	P	Power 1.2V
49	VDDC_PLL	P	Power 1.2V
50	VSS_PLL	P	Ground
51	VSS_PLL	P	Ground
52	XTAL_OUT	O	Crystal output
53	XTAL_IN	I	Crystal input
54	VDDH	P	Digital power 3.3V
55	VSS	P	Digital power ground
56	VDDC	P	Digital core power 1.2V
57	VDDH	P	Digital power 3.3V
58	VSS	P	Digital power ground
59	VDDC	P	Digital core power 1.2V
60	RES ETN	I	Global reset, active low
61	MCLK	O	Master clock for sensor
62	P35 / SSDA	B	General purpose IO Master I2C Bus : SDA
63	P34 / SSCK	B	General purpose IO Master I2C clock
64	P33 / I2S_LRCK	B	General purpose IO Audio serial interface channel clock
65	P32 / I2S_BCK	B	General purpose IO Audio serial interface bit clock

66	P36 / I2S_ADCDAT	B	General purpose IO
			ADC digital audio data output
67	TEST		Test Mode
68	P11 / iSDA	B	General purpose IO
			iP597x Slave I2C Data
69	P12 / MCU_MOSI / I2S_CLK12M	B	General purpose IO
			iP597x SPI MOSI
			Audio serial interface 12Mhz clock input
70	P13 / MCU_MISO / H264_DAT0	B	General purpose IO
			iP597x SPI MISO
			H264 SPI Data output
71	P14 / MCU_SCK / H264_SCK0	B	General purpose IO
			iP597x SPI Clock
			H264 SPI clock input
72	P15 / MCU_CS / H264_CS0	B	General purpose IO
			iP597x SPI Chip select
			H264 SPI CS input
73	P16 / H264_EMPTY	B	General purpose IO
			H264 SPI Empty Signal Output
74	P17 / H264_AUDIO	B	General purpose IO
			H264 SPI Audio Signal Output
75	VSS	P	Digital power ground
76	VDDQH	P	SDRAM Power 3.3V
77	VDDQH	P	SDRAM Power 3.3V
78	VSS	P	Digital power ground
79	VDDC	P	Digital core power 1.2V
80	VSS	P	Digital power ground
81	P30 / RX / I2S_DACDAT		General purpose IO
			UART RX
			DAC digital audio data input
82	P31 / TX	B	General purpose IO
			UART TX
83	P03 / FSPI_CS / H264_CS1	B	General purpose IO
			External Serial Flash chip select
			H264 SPI CS input
84	P00 / FSPI_MISO / H264_MISO1		General purpose IO
			External Serial Flash data input
			H264 SPI Data output
85	P01 / FSPI_MOSI	B	General purpose IO
			External Serial Flash data output
86	P02 / FSPI_SCK / H264_SCK1	B	General purpose IO
			External Serial Flash clock output
			H264 SPI clock input
87	D1		Sensor Data : D1
88	D0		Sensor Data : D0

Registers List

If the customers access registers through I2C, the register address are only two bytes. If the customers access registers through USB, the register address are four bytes.

For Bank 0x7x, the address on USB is 0x00027xYY.

For Bank 0x01, the address on USB is 0x000100YY.

◆ **Interrupt Control**

Bank	Add.	Name	bit	Att.	Describtion		Def.
0x70	0xEF	aoe_irq_maskn	b7	RW		Set to enable empty irq of the audio-out buffer	0x0
		aof_irq_maskn	b6	RW		Set to enable full irq of the audio-out buffer	0x0
		aie_irq_maskn	b5	RW		Set to enable empty irq of the audio-in buffer	0x0
		aif_irq_maskn	b4	RW		Set to enable full irq of the audio-in buffer	0x0
		ch0_firq_maskn	b3	RW		Set to enable full irq of the image input buffer of the ch0	0x0
		ch1_firq_maskn	b2	RW		Set to enable full irq of the image input buffer of the ch1	0x0
		jsta_irq_maskn	b1	RW		Set to enable JPEG stream start irq	0x0
		jend_irq_maskn	b0	RW		Set to enable JPEG stream end irq	0x0
0x70	0xF0	imask_encint	b7	RW		Set to enable H264 encoder irq	0x0
		imask_nal	b6	RW		Set to enable H264 NAL irq	0x0
		irq_vs_mode	b5-4	RW	0:	Front porch irq mode of the image VSYNC	0x0
					1:	Back porch irq mode of the image VSYNC	
					2:	Edge irq mode of the image VSYNC	
					3:	Reserved	
		hgop_irq_maskn	b3	RW		Set to enable H264 GOP-ready irq	0x0

		mot_irq_maskn	b2	RW		Set to enable motion detection irq	0x0
		sif_irq_maskn	b1	RW		Set to enable sif irq	0x0
		vs_irq_maskn	b0	RW		Set to enable VSYNC irq	0x0
0x70	0xF1	irq_encint	b7	RW		H264 encoder flag	0x0
		irq_streamnal	b6	RW		H264 NAL flag	0x0
		irq_stream	b5	RW		H264 GOP-ready flag	0x0
		irq_jsta	b4	RW		JPEG stream start flag	0x0
		irq_jend	b3	RW		JPEG stream end flag	0x0
		irq_mot	b2	RW		Motion detection flag	0x0
		irq_sif	b1	RW		SIF controller flag	0x0
		irq_vs	b0	RW		VSYNC flag	0x0

◆ **Test Control**

Bank	Add.	Name	bit	Att.	Describtion	Def.
0x70	0x00	cust_reg0	b7-0	RW	Customized registers #0	0x0
0x70	0x01	cust_reg1	b7-0	RW	Customized registers #1	0x0
0x70	0x02	cust_reg2	b7-0	RW	Customized registers #2	0x0
0x70	0x03	cust_reg3	b7-0	RW	Customized registers #3	0x0
0x70	0x04	cust_reg4	b7-0	RW	Customized registers #4	0x0
0x70	0x05	cust_reg5	b7-0	RW	Customized registers #5	0x0
0x70	0x06	cust_reg6	b7-0	RW	Customized registers #6	0x0
0x70	0x07	cust_reg7	b7-0	RW	Customized registers #7	0x0

Bank	Add.	Name	bit	Att.	Describtion		Def.
0x70	0xF2		b7-6			Reserved	
		ptgen_type	b5-4	RW	0:	Color bar pattern	0x0
					1:	Single color pattern	
					2:	Flow number pattern	
					3:	Reserved	
			b3-2			Reserved	
		ptgen_dyn	b1	RW		Set to change pattern dynamically	0x0
		ptgen_en	b0	RW		Set to enable built-in pattern	0x0
	0xF3	ptgen_yg	b7-0	RW		The luma of the single color pattern	0x16
	0xF4	ptgen_cb	b7-0	RW		The chroma of the single color pattern	0x80
	0xF5	ptgen_cr	b7-0	RW		The chroma of the single color pattern	0x80
	0xF6		b7-6			Reserved	
		ptgen_frate	b5-0	RW		Frame rate setting	0x21

◆ Clock Control

Bank	Add.	Name	bit	Att.	Describtion		Def.
0x70	0x08	cfa_eq_mclk	b7	RW	0:	cfaclk freq. is equal to the half mclk freq.	0x0
					1:	cfaclk freq. is equal to the mclk freq.	
		cfa_int_en	b6	RW	0:	Apply the sensor clock to be the cfa clock	0x0
					1:	Apply the internal clock to be the cfa clock	
		cfa_clk_sel	b5	RW	0:	cfa clock source selection from sensor PCLK	0x0
					1:	cfa clock source selection from sampled PCLK	
		cfa_clk_ph	b4	RW		cfa clock phase selection	0x0
			b3	RW		Reserved	
		mas_src_sel	b2	RW	0:	MCLK source selection from phy240	0x0
					1:	MCLK source selection from pll output	
		mas_trig	b1	RW		Set to trigger mclk setting	0x0
		mas_clken	b0	RW		MCLKEN, Set to enable master clock to sensor	0x0
0x70	0x09	mas_dplln2	b7-4	RW		MCLK = (CLKBASE)/(DPLLN1+1)/(2^(DPLLN2))	0x0
		mas_dplln1	b3-0	RW			0x6
0x70	0x0A	pel_ph_sel	b7-5	RW		Phase selection when sampling input PCLK	0x0
			b4			Reserved	
		ahb_dplln2	b3-2	RW		AHBCLK = (CLKBASE)/(DPLLN1+1)/(2^(DPLLN2))	0x0
		ahb_dplln1	b1-0	RW			0x0

0x70	0x0B		b7			Reserved	
		ahb_hclkinv	b6	RW		Set to inverse ahb_hclk	0x0
		dac_clksel	b5	RW	0:	Select DAC output clock	0x0
					1:	Select ahb_hclk	
		adc_clksel	b4	RW	0:	Select ADC output clock	0x0
					1:	Select ahb_hclk	
		sdram_dqisel	b3	RW	0:	Select dqi data directly	0x0
					1:	Select dqi data sampled by ahb_hclk	
		sif_clk_sel	b2-1	RW	0:	1MHz	0x0
					1:	500KHz	
					2:	250KHz	
		*Based on PLL=162MHz			3:	125KHz	
		audclk_sel	b0	RW	0:	Audio clock is from xtal clock	0x0
					1:	Audio clock is from PHY output 12MHz clock	
0x70	0x0C	sdr_clk_ph1inv	b7	RW		Set to inverse output sdr_clk	0x0
		sdr_clk_ph1sel	b6-4	RW	0:	Phase0 of the output sdr_clk	0x0
					1:	Phase1 of the output sdr_clk	
					2:	Phase2 of the output sdr_clk	
					3:	Phase3 of the output sdr_clk	
		sdr_clki_ph1inv	b3	RW		Set to inverse input sdr_clki	0x0

		sdr_clki_ph1sel	b2-0	RW	0:	Phase0 of the input sdr_clki	0x0
					1:	Phase1 of the input sdr_clki	
					2:	Phase2 of the input sdr_clki	
					3:	Phase3 of the input sdr_clki	
0x70	0x2E	sdr_clk_ph2inv	b7	RW		Set to inverse sdr_clk in the stage2	0x0
		sdr_clk_ph2sel	b6-4	RW		Phase selection of the sdr_clk in the stage2	0x0
		sdr_clki_ph2inv	b3	RW		Set to inverse sdr_clki in the stage2	0x0
		sdr_clki_ph2sel	b2-0	RW		Phase selection of the sdr_clki in the stage2	0x0
0x70	0x2F	sdr_clk_ph3inv	b7	RW		Set to inverse sdr_clk in the stage3	0x0
		sdr_clk_ph3sel	b6-4	RW		Phase selection of the sdr_clk in the stage3	0x0
		sdr_clki_ph3inv	b3	RW		Set to inverse sdr_clki in the stage3	0x0
		sdr_clki_ph3sel	b2-0	RW		Phase selection of the sdr_clki in the stage3	0x0
0x70	0xF8		b7-6			Reserved	
		pll_dm	b5-0	RW		PLL DM parameter	0x01
0x70	0xF9		b7			Reserved	
		pll_dn	b6-0	RW		PLL DN parameter	0x1b
0x70	0xFA		b7-3			Reserved	
		pll_dp	b2-0	RW		PLL DP parameter	0x01
0x70	0xFB		b7-5			Reserved	
		pllc_ok	b4	R		Set by HW. to indicate the PLL parameters updated ok.	0x0

			b3-2			Reserved	
		pll_bypass	b1	RW		Set to bypass PLL	0x0
		pll_setpar	b0	RW		Set to update PLL parameters	0x0
0x73	0x06	sdc_dplln2	b7-4	RW		SDCLK = (CLKBASE)/(DPLLN1+1)/(2^(DPLLN2))	0x5
		sdc_dplln1	b3-0	RW			0xf
0x71	0x0F		b7-2			Reserved	
		encm_ccon	b1-0	RW		H264 MCU clock selection	0x0

◆ **Audio Control**

Bank	Add.	Name	bit	Att.	Describtion	Def.
0x70	0x1A	audi_comp_en	b7	RW	Set to enable input audio compensation algorithm	0x0
		audi_adata_err	b6	R	Internal audio testing flag	0x0
		audi_com_per	b5-0	RW	Input audio compensation period	0x24
0x70	0x1B	audo_comp_en	b7	RW	Set to enable output audio compensation algorithm	0x0
			b6		Reserved	
		audo_com_per	b5-0	RW	Output audio compensation period	0x24
0x70	0x1C	audi_upktsize[7:0]	b7-0	RW	UDMA packet size of the input audio	0x00
0x70	0x1D	audi_upktsize[10:8]	b2-0	RW		0x0
0x70	0x38	codec_master	b7	R	CODEC I2S master mode indicator	
			b6		Reserved	
		codec_porten	b5	RW	Set to turn on the CODEC stand-alone mode	0x0
		codec_tmic	b4	RW	CODEC input	0x0
		codec_tconfig	b3	RW	CODEC input	0x0
		codec_tslave	b2	RW	CODEC input	0x0
		codec_tpllbyp	b1	RW	CODEC input	0x0
		codec_rstn	b0	RW	CODEC input	0x0
0x70	0x98		b7-4			
		audi_smp	b3-0	RW	Audio-in re-sampling period	0x0

◆ **USB Control**

Bank	Add.	Name	bit	Att.		Describtion	Def.
0x70	0x0F		b7-1			Reserved	
		u_vbus	b0	RW		Set to enable USB bus	0x0
0x70	0x39		b7-5			Reserved	
		uvc_sof_mode	b4	RW	0:	Count sof number 1-by-1 for the UVC	0x0
					1:	Count sof number 1-by-3 for the UVC	
		hbw_level1_sel	b3-2	RW		Check point of the LV1 to decide how many packets should be transmit in the USB HBW mode	0x2
		hbw_level0_sel	b1-0	RW		Check point of the LV0 to decide how many packets should be transmit in the USB HBW mode	0x1
0x70	0x3A	stc_base_div	b7-0	RW		UVC STC counter base number	0xa6

◆ Image Control

Bank	Add.	Name	bit	Att.		Describtion	Def.
0x70	0x10	img_reset	b7	RW		Set to reset image	0x0
		img_trig				Set to trigger image control parameter updating	0x0
		img_ptn	b5-4	RW	0:	Input YUV array pattern, uyvy	0x0
					1:	Input YUV array pattern, vyuy	
					2:	Input YUV array pattern, yuyv	
					3:	Input YUV array pattern, yvyu	
		img_hs_p	b3	RW		Set to inverse HSYNC	0x0
		img_vs_p	b2	RW		Set to inverse VSYNC	0x0
		img_ccir_en	b1	RW		Set to enable ccir656 raw data input	0x0
		img_en	b0	RW		Set to enable image processor	0x0
0x70	0x11	img_width[7:0]	b7-0	RW		Image width	0x7f
0x70	0x12	img_width[10:8]	b2-0	RW			0x2
0x70	0x13	img_height[7:0]	b7-0	RW		Image Height	0xdf
0x70	0x14	img_height[8]	b0	RW			0x1
0x70	0x15	img_pstart[7:0]	b7-0	RW		Image pixel start	0x00
0x70	0x16	img_pstart[10:8]	b2-0	RW			0x0
0x70	0x17	img_lstart[7:0]	b7-0	RW		Image line start	0x00
0x70	0x18	img_lstart[8]	b0	RW			0x0

0x70	0x50	res_mode_ch0	b7-6	RW	0:	Apply VGA mode on the channel0	0x0
					1:	Apply QVGA mode on the channel0	
					2:	Apply QQVGA mode on the channel0	
					3:	Apply VGA mode on the channel0	
		yuv_frid_acc_ch0	b4	R		The writing frame ID on the channel0	0x0
		chan0_en	b3	RW		Set to enable channel0	0x0
		yuv0_wrhburst	b2-0	RW		AHB burst mode selection on the channel0	0x5
0x70	0x70	res_mode_ch1	b7-6	RW	0:	Apply VGA mode on the channel1	0x0
					1:	Apply QVGA mode on the channel1	
					2:	Apply QQVGA mode on the channel1	
					3:	Apply VGA mode on the channel1	
		yuv_frid_acc_ch1	b4	R		The writing frame ID on the channel1	0x0
		chan1_en	b3	RW		Set to enable channel1	0x0
		yuv1_wrhburst	b2-0	RW		AHB burst mode selection on the channel1	0x5
0x70	0x90		b7-2			Reserved	
		irsp_mode	b1	RW	0:	Choose one frame between irsp_frate frames	0x0
					1:	Drop one frame between irsp_frate frames	
		irsp_bypass	b0	RW		Set to bypass image frame rate controller	0x1
0x70	0x91	irsp_frate	b7-0	RW		Frame period for frame the rate controller	0x00

◆ **ISP Control**

Bank	Add.	Name	bit	Att.	Describtion	Def.
0x70	0xAA	blur_func	b7-5	RW	Blur level	0x0
		blur_enable	b4	RW	Set to enable blur function	0x0
		denois_func	b3-1	RW	Noise reduction level	0x0
		denois_en	b0	RW	Set to enable noise reduction function	0x0
	0xAB		b7-6		Reserved	
		imeh_strength	b5-1	RW	Enhancement level	0x0
		imeh_en	b0	RW	Set to enable image enhancement function	0x0
	0xAC	imeh_coring_th	b7-4	RW	Coring level	0x0
		imeh_high_scale	b3-2	RW	High level scale	0x0
		imeh_low_scale	b1-0	RW	Low level scale	0x0

◆ Motion Control

Bank	Add.	Name	bit	Att.	Describtion		Def.
0x70	0x82	mblknum_thr[7:0]	b7-0	RW		Tthe motion block number threshold.	0x00
0x70	0x83		b7-2			Reserved	
		mblknum_thr[9:8]	b1-0	RW		The motion block number threshold.	0x0
0x70	0x84		b7-4			Reserved	
		mblk_allen	b3	RW		Set to enable all motion block.	0x0
		mblkprg_mode	b2	RW	0:	MBLK address will be increased automatically when programming motion block	0x0
					1:	Fixed MBLK address when programming motion block	
		mblkprg_en	b1	RW		Set to program motion block	0x0
		mot_en	b0	RW		Set to enable motion detection	0x0
0x70	0x85	mot_frame_gap	b7-0	RW		Frame interval for the motion detection	0x00
0x70	0x87		b7			Reserved	
		mblk_adr_s1	b6-0	RW		The initial address of the motion block for writing and reading	
0x70	0x88	mblk_rdout	b7-0	W		Writing MBDAT to motion block memory.	0x00
				R		Reading MBDAT from motion block memory	
0x70	0x89		b7			Reserved	
		mvec_rd_adr	b6-0	RW		The initial address to read block motion indicator.	0x00
0x70	0x8A	hrd_mvec	b7-0	R	0:	Image Block is freeze.	

					1:	Image Block motion is detected.	
0x70	0x8B	mot_dec_out	b7	RW		Set by HW when frame motion is detected	0x0
						This bit should be reset by SW	
			b6			Reserved	
		h_fhold_mdat	b5	RW		Set to hold motion data memory always.	0x0
		h_fhold_mvec	b4	RW		Set to hold motion indicator memory always	0x0
		h_hold_mvec	b3	RW		Set to hold motion indicator memory when motion is detected	0x0
		h_hold_mdat	b2	RW		Set to hold motion data memory when motion is detected	0x0
		hrd_mdat_mode	b1	RW	0:	Motion data address will be increased automatically	0x0
					1:	Motion data address will be fixed as mvec_rd_adr(0x7089)	
		hrd_mvec_mode	b0	RW	0:	Motion indicator address will be increased automatically	0x0
					1:	Motion indicator address will be fixed as mvec_rd_adr(0x7089)	
0x70	0x8C	mdat_rd_adr[7:0]	b7-0	RW		The initial address to read motion blocks data	0x00
0x70	0x8D		b7-2			Reserved	
		mdat_rd_adr[9:8]	b1-0	RW		The initial address to read motion blocks data	0x0
0x70	0x8E	hrd_mdat	b7-0	R		Motion blocks data average	
0x70	0x8F	mblk_thr	b7-0	RW		Block motion threshold for the motion detection	0xff

Fig. Motion block enable memory, 75(40/8x15) addresses only for VGA

Fig. Motion block configuration 16x32 only for VGA, 40x15 motion blocks for VGA

◆ **Raw Data control**

Bank	Add.	Name	bit	Att.	Describtion		Def.
0x70	0x1E	raw_upktsize[7:0]	b7-0	RW		UDMA packet size of the image raw data	0x00
0x70	0x1F	raw_hbwnum	b5-4	RW	0:	Apply one time raw_upktsize for the USB iso packet	0x0
					1:	Apply one time raw_upktsize for the USB iso packet	
					2:	Apply two times raw_upktsize for the high bandwidth iso packet	
					3:	Apply three times raw_upktsize for the high bandwidth iso packet	
		raw_upktsize[11:8]	b3-0	RW		UDMA packet size of the image raw data	0x4
0x70	0x45	raw_ufifonum	b7-4	RW		USB fifo number for the raw data	0x0
			b3			Reserved	
		raw_uvc_en	b2	RW		Set to enable UVC protocol on the raw data	
		raw_bufchsel	b1	RW	0:	Select image channel 0	0x0
					1:	Select image channel 1	
		raw_udma_en	b0	RW		Set to enable UDMA raw data function	0x0

◆ **JPEG control**

Bank	Add.	Name	bit	Att.	Describtion		Def.
0x70	0x3B	jpeg_upktsize[7:0]	b7-0	RW		UDMA packet size of the JPEG stream data	0x00
0x70	0x3C	jpeg_hbwnum	b5-4	RW	0:	Apply one time jpeg_upktsize for the USB iso packet	0x0
					1:	Apply one time jpeg_upktsize for the USB iso packet	
					2:	Apply two times jpeg_upktsize for the high bandwidth iso packet	
					3:	Apply three times jpeg_upktsize for the high bandwidth iso packet	
		jpeg_upktsize[11:8]	b3-0	RW		UDMA packet size of the image JPEG stream data	0x4
0x70	0x43	jpeg_ufifonum	b7-4	RW		USB fifo number for the JPEG stream accessing	0x0
			b3			Reserved	0x0
		jpeg_uvc_en	b2	RW		Set to enable UVC protocol on the JPEG stream	0x0
			b1			Reserved	0x0
		jpeg_udma_en	b0	RW		Set to enable UDMA JPEG function	0x0
0x70	0x9F	jpeg_strbuf_addr[7:0]	b7-0	RW		JPEG stream buffer start address in the SDRAM	0x00
0x70	0xA0	jpeg_strbuf_addr[15:8]	b7-0	RW		JPEG stream buffer start address in the SDRAM	0xa8
0x70	0xA1	jpeg_sizbuf_addr[7:0]	b7-0	RW		JPEG size buffer start address in the SDRAM	0x00
0x70	0xA2	jpeg_sizbuf_addr[15:8]	b7-0	RW		JPEG size buffer start address in the SDRAM	0xa0
0x70	0xA3	jpeg_buf_num[7:0]	b7-0	RW		JPEG stream buffer number in the SDRAM	0x10
0x70	0xAE	jpeg_buf_numleft	b7-0	RW		JPEG stream number left in the SDRAM	0x02
0x72	0xB9	qscale	b7-4	RW		Quality scale function for JPEG channel	0x3

		jch_sel	b3	RW		Image channel selection	0x0
		j_mono_en	b2	RW		Set Mono. Image for JPEG channel	0x0
		uvchead_en	b1	RW		Set to send UVC head	0x0
		jpeg_en	b0	RW		Set to enable JPEG encoder	0x0
0x72	0xBA	jqqvga_en	b7	RW		Set to encode QQVGA image	0x0
		jqvga_en	b6	RW		Set to encode QVGA image	0x0
			b5-4			Reserved	
		header_en	b3	RW		Set to enable JPEG full header with the encoded stream	0x0
		jsize_en	b2	RW		Set to send JPEG size in the header	0x0
		det_mot	b1	RW		This bi will be set when the motion is detected	0x0
		jmot_en	b0	RW		Set to send motion detection flag in the header	0x0
0x72	0xBB	jwid[7:0]	b7-0	RW		JPEG image width	0x7f
0x72	0xBC		b7-2			Reserved	
		jwid[9:8]	b1-0	RW		JPEG image width	0x2
0x72	0xBD	jhei[7:0]	b7-0	RW		JPEG image height	0xdf
0x72	0xBE		b7-1			Reserved	
		jhei[8]	b0	RW		JPEG image height	0x1
0x72	0xC0	jbuf_refer_sel	b7-6	RW	0:	Free-run mode	0x0
					1:	Refer to UDMA buffer only	
					2:	Refer to SDMA buffer only	

					3:	Refer to both UDMA and SDMA buffer	
			b5-2			Reserved	
		jselfsof	b1	RW		Set to enable internal sof counter	0x0
		jfrstn	b0	RW		Set to enable JPEG buffer	0x0

◆ H264 Encoder Control

Bank	Add.	Name	bit	Att.		Describtion	Def.
0x70	0x3D	h264_upktsize[7:0]	b7-0	RW		UDMA packet size of the H264 stream data	0x00
0x70	0x3E	h264_hbwnum	b5-4	RW	0:	Apply one time h264_upktsize for the USB iso packet	0x0
					1:	Apply one time h264_upktsize for the USB iso packet	
					2:	Apply two times h264_upktsize for the high bandwidth iso packet	
					3:	Apply three times h264_upktsize for the high bandwidth iso packet	
		h264_upktsize[11:8]	b3-0	RW		UDMA packet size of the image H264 stream data	0x4
0x70	0x40	h264_ufifonum	b7-4	RW		USB fifo number for the H264 stream accessing	0x0
			b3			Reserved	
		h264_uvc_en	b2	RW		Set to enable UVC protocol on the H264 stream	0x0
		h264_tgl_en	b1	RW		Set to enable UVC toggle bit for the H264 protocol	0x0
		h264_udma_en	b0	RW		Set to enable UDMA H264 function	0x0
0x70	0xFF	func_state	b7-0	RW		H264 Function statement	0x00
0x71	0x0D		b7-3			Reserved	
		hbuf_refer_sel	b2-0	RW	0:	Free-run mode	0x0
					1:	Refer to UDMA buffer only	
					2:	Refer to SDMA buffer only	
					3:	Refer to PDMA buffer only	
					4:	Refer to both UDMA and SDMA buffer	

					5:	Refer to both UDMA and PDMA buffer	
					6:	Refer to both SDMA and PDMA buffer	
					7:	Refer to all UDMA, SDMA and PDMA buffer	

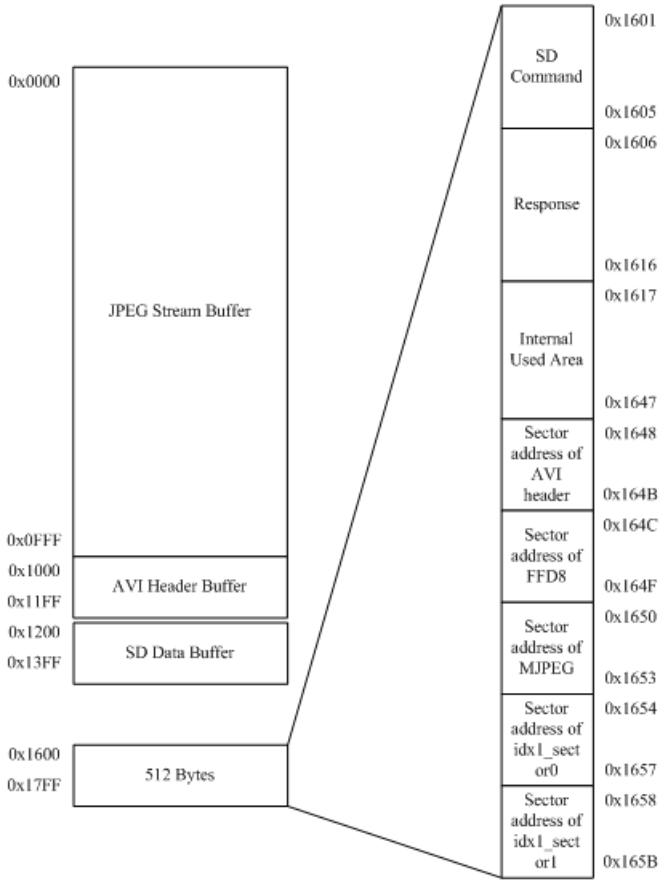


Fig. External Memory Mapping for the SDCard control

◆ **PDMA Control**

Bank	Add.	Name	bit	Att.	Describtion		Def.
0x70	0x51	pdma_abuf_afull	b7	R		Audio buffer full flag of the PDMA	
		pdma_abuf_empty	b6	R		Audio buffer empty flag of the PDMA	
		aud_pdma_mono	b5	RW		Set audio mono mode for the PDMA	0x0
		aud_pdma_en	b4	RW		Set to enable audio channel for the PDMA	0x0
		hspi_sck_sel	b3	RW		HSPI sck phase selection	0x0
		hspi_msb	b2	RW	0:	LSB mode for HSPI bus	0x0
					1:	MSB mode for HSPI bus	
		hspi_master	b1	RW	0:	Slave mode for HSPI bus	0x0
					1:	Master mode for HSPI bus	
		h264_pdma_en	b0	RW		Set to enable H264 channel for the PDMA	0x0
0x70	0x52	hspi_wait_num[15:8]	b7-0	RW			0x04
0x70	0x53	hspi_wait_num[7:0]	b7-0	RW			0x00
0x70	0x54	hspi_csn_num	b7-4	RW			0x1
		hspi_sck_num	b3-0	RW			0x1
0x70	0x55	hspi_dly_num	b7-0	RW			0x00
0x70	0x57		b7-3			Reserved	
		hspi_pktsize	b2-0	RW	0:	4 bytes	0x7
					1:	8 bytes	

					2:	16 bytes	
					3:	32 bytes	
					4:	64 bytes	
					5:	128 bytes	
					6:	256 bytes	
					7:	512 bytes	
0x70	0x59	h264_pktsize	b7-4	RW		The packet size to load H264 stream from SDRAM	0x2
						Packet_size=h264_pktsize*128	
		audi_pktsize	b3-0	RW		The packet size to load audio stream from SDRAM	0x1
						Packet_size=audi_pktsize*128	

◆ **RTDC Control**

Bank	Add.	Name	bit	Att.	Describtion		Def.
0x70	0xC9	char_space	b7-5	RW		The space between characters	0x0
		time24	b4	RW	0:	12 hours	0x0
					1:	24 hours	
		time_order	b3-1	RW		Display format order setting	0x0
		rtdc_en	b0	RW		Set to enable date and time display function	0x0
0x70	0xCA	rtdc_rom_sw	b7	RW	0:	Apply default rom for font	0x0
					1:	Apply osd rom for font	
		hide_time	b6	RW		Set to hide time display	0x0
		hide_date	b5	RW		Set to hide date display	0x0
		showpmam	b4	RW		Set to hide pm/am display	0x0
		tfont_scale_y	b3-2	RW		The height of the time font size	0x0
		tfont_scale_x	b1-0	RW		The width of the time font size	0x0
0x01	0x17	year[7:0]	b7-0	RW		Set year, BCD coding	0x06
0x01	0x15	month	b7-0	RW		Set month, BCD coding	0x01
0x01	0x14	date	b7-0	RW		Set date, BCD coding	0x20
0x01	0x13	hour	b7-0	RW		Set hour, BCD coding	0x05
0x01	0x12	min	b7-0	RW		Set min, BCD coding	0x30
0x01	0x11	sec	b7-0	RW		Set sec, BCD coding	0x30

0x01	0x19	Reserved	b7-1			Set as update new RTC	0x00
		bWriteRTC	b0	RW			
0x70	0xD2	time_locx	b7-0	RW		Set date pixel location	0x03
0x70	0xD3		b7			Reserved	
		time_locy	b6-0	RW		Set date line location	0x03
0x70	0xD4	time_locx1	b7-0	RW		Set time pixel location	0x28
0x70	0xD5	time_locy1	b7-0	RW		Set time line location	0x06
0x70	0xD6	rtd_y	b7-0	RW		Set luma of the time character	0x7a
0x70	0xD7	rtd_u	b7-0	RW		Set Chroma of the time character	0x48
0x70	0xD8	rtd_v	b7-0	RW		Set Chroma of the time character	0x3a
0x70	0xD9	rtdbg_y	b7-0	RW		Set luma of the time background	0x1a
0x70	0xDA	rtdbg_u	b7-0	RW		Set Chroma of the time background	0x48
0x70	0xDB	rtdbg_v	b7-0	RW		Set Chroma of the time background	0x3a
0x70	0xDC		b7	RW		Reserved	
		osdbg_tran	b6-4	RW		Set transparency of the osd background	0x0
			b3	RW		Reserved	
		rtdbg_tran	b2-0	RW		Set transparency of the time background	0x0
0x70	0xDD	osd_ack	b7	R		The hardware ack to indicate the finish of the write/read osd font memory	
			b6-2	RW		Reserved	
		prgen	b1	RW		Set to write/read osd font memory	0x0

		osden	b0	RW		Set to enable osd function	0x0
0x70	0xDE	grp1_locx	b7-0	RW		Set group1 pixel location	0x03
0x70	0xDF	grp2_locx	b7-0	RW		Set group2 pixel location	0x06
0x70	0xE0	grp3_locx	b7-0	RW		Set group3 pixel location	0x09
0x70	0xE1	grp4_locx	b7-0	RW		Set group4 pixel location	0x0c
0x70	0xE2	grp1_locy	b7-0	RW		Set group1 line location	0x13
0x70	0xE3	grp2_locy	b7-0	RW		Set group2 line location	0x26
0x70	0xE4	grp3_locy	b7-0	RW		Set group3 line location	0x39
0x70	0xE5	grp4_locy	b7-0	RW		Set group4 line location	0x4c
0x70	0xE6	osd_y	b7-0	RW		Set luma of the osd character	0x7a
0x70	0xE7	osd_u	b7-0	RW		Set Chroma of the osd character	0x48
0x70	0xE8	osd_v	b7-0	RW		Set Chroma of the osd character	0x3a
0x70	0xE9	osdbg_y	b7-0	RW		Set luma of the osd background	0x1a
0x70	0xEA	osdbg_u	b7-0	RW		Set Chroma of the osd background	0x48
0x70	0xEB	osdbg_v	b7-0	RW		Set Chroma of the osd background	0x3a
0x70	0xEC	osd_dat	b7-0	RW		The Entry Point to Write/Read OSD Font Memory 1. When write/read osd font memory, the memory address will be increased automatically by hardware. 2. For each data writing/reading, the ack at bit7 of the 0xdd should be checked before the next writing/reading procedure.	0x00

◆ **Serial I/F control**

Bank	Add.	Name	bit	Att.	Describtion		Def.
0x70	0x47	sif_sel	b7-6	RW	0:	Disable	0x0
					1:	Sensor I2C	
					2:	CODEC I2C	
					3:	Reserved	
			b5			Reserved	
		sif_stop	b4	RW		Generate the stop signal during the reading task	0x0
			b3-2			Reserved	
		adr_mode	b1	RW	0:	8-bit mode address	0x0
					1:	16-bit mode address	
		i2c_mode	b0	RW	0:	8-bit mode data	0x0
					1:	16-bit mode data	
0x70	0x48		b7-5			Reserved	
		sif_nak	b4	RW		Set by HW to indicate the SIF time out state	0x0
						This bit should be clear by SW.	
			b3			Reserved	
		sif_txv	b2	RW		Trigger to write at vsync front edge.	0x0
						This bit will be reset when the writing sequence is done.	
		sif_rx	b1	RW		Set to trigger SIF reading sequence.	0x0

						This bit will be reset when the writing sequence is done.	
		sif_tx	b0	RW		Set to trigger SIF writing sequence.	0x0
						This bit will be reset when the writing sequence is done.	
0x70	0x49		b7			Reserved	
		sif_device_adr	b6-0	RW		I2C device address	0x0
0x70	0x4A	sif_data_adr1	b7-0	RW		I2C data address1	0x0
0x70	0x4B	sif_data_adr2	b7-0	RW		I2C data address2	0x0
0x70	0x4C	sif_tx_data1	b7-0	RW		I2C transmitted data1	0x0
0x70	0x4D	sif_tx_data2	b7-0	RW		I2C transmitted data2	0x0
0x70	0x4E	sif_rx_data1	b7-0	R		I2C received data1	
0x70	0x4F	sif_rx_data2	b7-0	R		I2C received data2	
0x70	0xC8		b7			Reserved	
		codec_i2c_addr	b6-0	RW		CODEC I2C Address	0x5a

◆ **H264 control**

Bank	Add.	Name	bit	Att.	Describtion	Def.
0x04	0x31	LSB_GOPL	b7-0	RW	LSB of Group Length	0x1E
0x04	0x32	MSB_GOPL	b7-0	RW	MSB of Group Length	0x00
0x04	0x22	LSB_IRate	b7-0	RW	LSB of I frame rate	0x0A
0x04	0x23	MSB_IRate	b7-0	RW	MSB of I frame rate	0x00
0x04	0x00	D0_LastPic	b7-0	RW	Last Picture b[7:0]	0x1D
0x04	0x01	D1_LastPic	b7-0	RW	Last Picture b[15:8]	0x00
0x04	0x02	D2_LastPic	b7-0	RW	Last Picture b[23:16]	0x00
0x04	0x03	D3_LastPic	b7-0	RW	Last Picture b[31:24]	0x00
0x04	0x26	D0_BitRate	b7-0	RW	Bit Rate b[7:0]	0x80
0x04	0x27	D1_BitRate	b7-0	RW	Bit Rate b[15:8]	0x84
0x04	0x28	D2_BitRate	b7-0	RW	Bit Rate b[23:16]	0x1E
0x04	0x29	D3_BitRate	b7-0	RW	Bit Rate b[31:24]	0x00
0x04	0x2A	BitRate_Mode	b7-0	RW	1: Set as constant bit rate 0: Set as fix quality	0x01
0x04	0x34	Init_Quality	b7-0	RW	Initial quality. 0x0A~0x33 are valid.	0x1A
0x04	0x38	I_Quailtiy	b7-0	RW	I frame quality when register 0x042A is 0x00	0x00
0x01	0x0E	bH264_Update	b0	RW	Write 0x01 to update all the registers about H264.	0x00

Recommanded Operation Conditions

Parameter	Limit			Unit
	Min	Typ	Max	
Core DC Supply Voltage	1.08	1.2	1.32	Volt
I/O DC supply Voltage	3.0	3.3	3.6	Volt
Temperature	0	25	125	°C

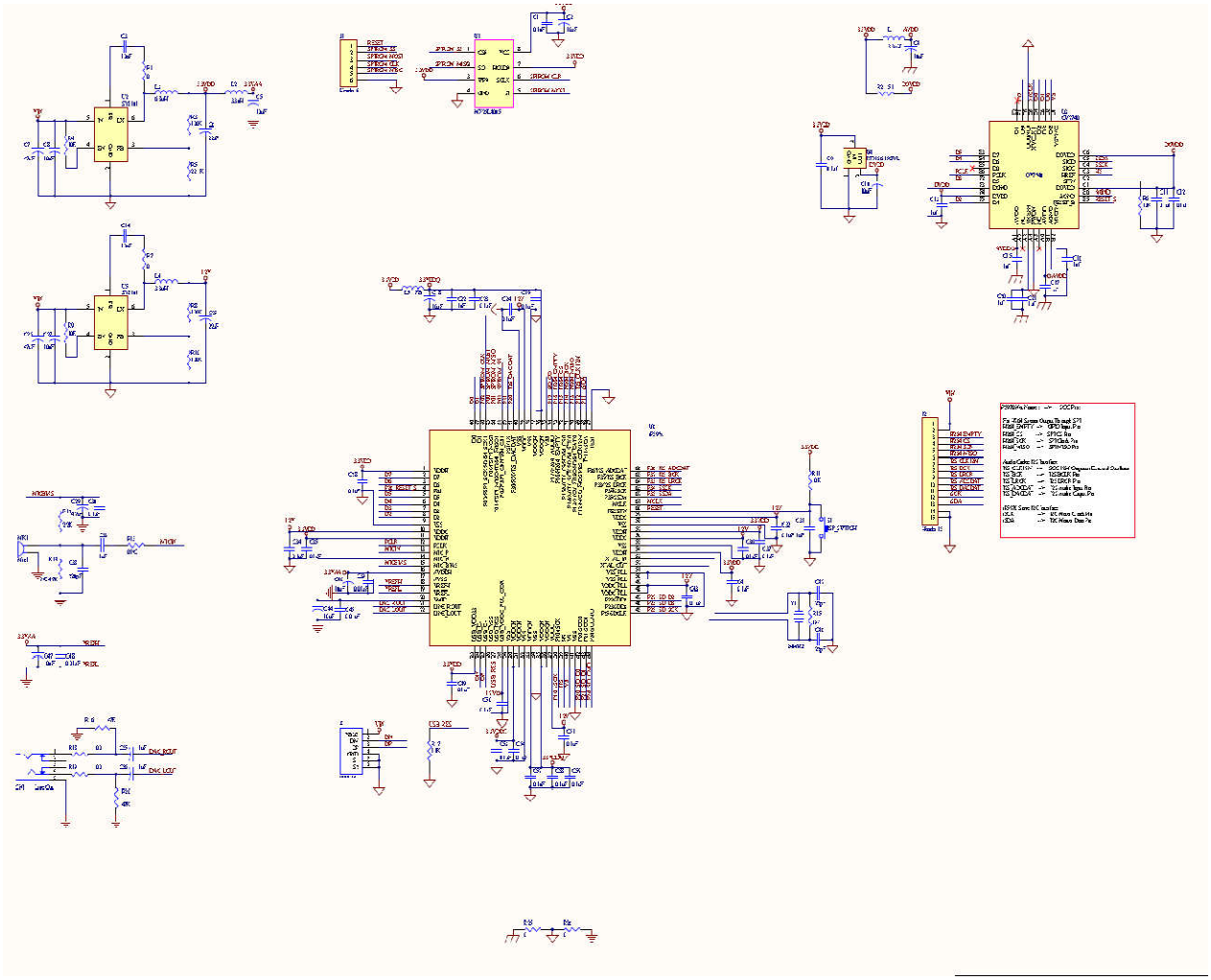
DC Electrical Characteristics

Parameter	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
Low level Input Voltage	V_{IL}			0.8	V	LVTTL/CMOS interface
High level Input Voltage	V_{IH}	2.0			V	LVTTL/CMOS interface
Low level Output Voltage	V_{OL}			0.4	V	IOL = 4, 8, 24mA
High level Output Voltage	V_{OH}	2.4			V	IOH = -4, -8, -24mA
Input Current	I_I	-10		10	μA	Vdd = MAX, 0V ≤ Vin ≤ 3.6V
Input Current with pull-down		40		160	μA	Vin = Vd
Input Current with pull-up		-160		40	μA	Vin=0
Input pull-up resistance	RPU	33	49	84	kΩ	VIN =0
Input pull-down resistance	RPD	29	51	101	kΩ	VIN =VDDH

AC Electrical Characteristics

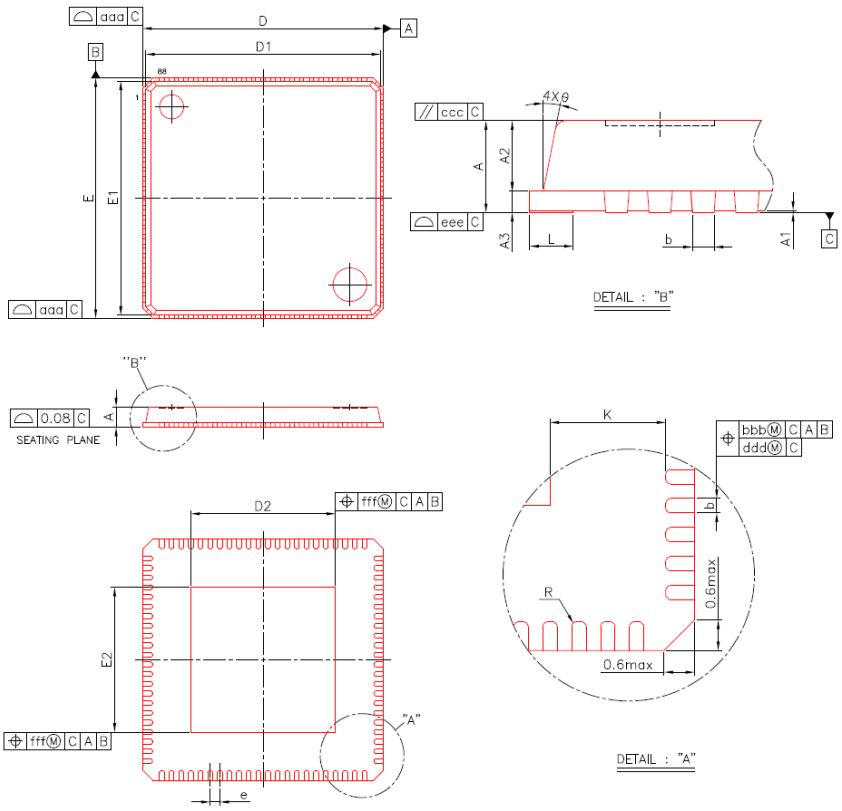
Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Sensor Master Clock	mclk			27	MHz
Sensor Pixel Clock	pclk			27	MHz
Crystal Input	xtalin			24	MHz

Reference Schematic of SPI Camera : (Ver. 1.1)



Package Information

- **88 Pin QFN**



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	10.00 BSC			0.394 BSC		
D1/E1	9.75 BSC			0.384 BSC		
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.075	---	---	0.003	---	---
K	0.20	---	---	0.008	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

L/F	Exposed Pad Size					
	D2/E2 (mm)			D2/E2 (inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
-						
②	6.75	6.90	7.05	0.266	0.272	0.278

TITLE : 88LD QFN (10X10 mm) PACKAGE OUTLINE			
L/F MATERIAL : A194 FH			
APPR.	L.C.CHIANG	DWG NO.	CE088-SW1
ENG.	Albert Lee David Gwo	REV NO.	D
QM.	Lee-Ying Chang	PRODUCT CODE	CE0881A,CE0881B KB0881A,KB0881B
CHK.	Y.Y.Lai	DATE	04/02/'07